REMARKS

By the present amendment claims 1 and 13 have been amended to clarify the invention.

Claims 1-20 remain pending in the application.

In the Final Office Action, the Examiner rejected claims 1-12 under 35 U.S.C. §112 as being indefinite.

Claims 1, 6-9, 12-13, 17 and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Number 5,640,525 to Yumoto et al.

Claims 2-5 and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yumoto et al. in view of U.S. Patent Number 6,530,011 to Choquette.

Claims 11 and 19 were rejected under 35 U.S.C.§103(a) as being unpatentable over Yumoto et al. in view of Hennessy.

Claims 10 and 18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the arguments that follow, Applicant respectfully traverses the Examiner's rejection of claims 1-9, 11-27 and 19-20.

Rejection Under 35 U.S.C. §112, second paragraph

The Examiner rejected claims 1-12 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Although the Examiner rejected claims 1-12 (see page 2, paragraph 6 of the Office Action), the Examiner asserted that claims 1 and 13 recite the limitation "each constant address," which is insufficient antecedent basis for the limitation in the claim.

Applicants respectfully request that the Examiner clarify the claims that are rejected under 35 U.S.C. §112, second paragraph. Applicants also respectfully submit that claims 1 and 13 have been amended to clarify the invention. Accordingly, Applicants respectfully request that that the rejection of claims 1 and 13 should be withdrawn.

Rejection Under 35 U.S.C. §102(b)

The Examiner rejected claims 1, 6-9, 12-13, 17 and 20 under 35 U.S.C. §102(b) as being anticipated by Yumoto et al. The rejection is respectfully traversed.

Applicants amended claim 1 recites: an execution control apparatus of a data driven information processor, said execution control apparatus comprising: a handled instruction that includes N + 2 (N is an arbitrary integer of at least 1) inputs, in which one of the inputs is a constant when an instruction has N + 2 inputs; an instruction decoder that decodes an instruction in an input packet and outputs a number of inputs required for said instruction; a waiting storage region including a waiting data storage region that

can store N waiting data in each waiting data address, and a data valid flag storage region that stores a data valid flag for each waiting data address, said data valid flag indicating whether the N waiting data stored in said each waiting data address is respectively valid or invalid; a constant storage device including a region that stores a constant, and a constant valid flag storage region that stores a constant valid flag representing whether a constant stored in a plurality of constant addresses are valid or invalid; a constant readout unit that accesses said constant storage region according to the constant address information included in the input packet to read out a constant and a constant valid flag from a relevant constant address in said constant storage region; a waiting operation determination unit that determines a hash address by a hash calculation from contents of the input packet, selects one predetermined way out of a plurality of predetermined ways of processing waiting data, outputs a select signal for the predetermined way of processing waiting data depending upon a combination of a data valid flag for said determined hash address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting data storage region, and updates the data valid flag for said hash address based on the select predetermined way of processing waiting data; and a waiting region access unit being responsive to said select signal to implement a waiting process corresponding to said select signal.

The Examiner alleged that Yumoto et al. discloses the recitations of claim 1, by referencing col. 7, lines 11-12 and referring to a data pair generation mechanism: interleave flag, address generation circuit, and data select circuit which is defined by the

Examiner as an address generation circuit that inherently generates or determines an address; referencing col. 4, lines 5-9 which is defined by the Examiner as showing that data from memory and the packet are check for hash collision which means that the addresses must be generated by a hash calculation; referencing col. 7, lines 12-15 which is defined by the Examiner as showing that one of a plurality of mechanisms for generating data is selected; referencing col. 4, lines 24-35 which is defined by the Examiner as showing that a packet is output based on the number of inputs and a valid flag for data from the matching memory; referencing col. 11, lines 44-47 which is defined by the Examiner as showing that the selection is based off of a VLD flag; referencing col. 10, lines 20-22 which is defined by the Examiner as being the valid flag of the constant; and referencing col. 4, lines 31-35 which is defined by the Examiner as showing that the valid data flag (PRE) is updated.

Applicants respectfully submit that Yumoto et al. does not disclose or teach all the claimed limitations of the present invention. Among other things, the reference does not disclose "a handled instruction that includes N + 2 (N is an arbitrary integer of at least 1) inputs, in which one of the inputs is a constant when an instruction has N + 2 inputs," as recited in amended claim 1.

Yumoto et al. disclose a firing control mechanism adapted (FC-adapted) 2-input instruction execution packet detection unit that detects whether an input packet is a 2-input instruction execution packet or not. The FC-adapted 2-input instruction execution packet detection unit generates a flag indicating whether an input packet is a 2-input instruction execution or not, and provides the flag to the firing control main processing

unit together with the required data in the input packet. Yumoto et al. further disclose that when a data packet is latched in a data latch, the FC-adapted 2-input instruction execution packet detection unit detects whether the packet is an FC-adapted 2-input instruction execution packet and generates a flag representing the determination results.

The FC-adapted 2-input instruction execution packet detection unit of Yumoto et al. for generating a flag indicating whether an input packet is a 2-input instruction execution or not merely determines the presence of a 2-input instruction execution and is not analogous to "a handled instruction that includes N + 2 (N is an arbitrary integer of at least 1) inputs, in which one of the inputs is a constant when an instruction has N + 2 inputs." Yumoto et al. merely detects whether an input packet is argument data of a 1-input or 2-input instruction. Moreover, there is nothing in the invention of Yumoto et al. that discloses an instruction that includes more than 2 inputs. In the present invention, the handled instruction includes N+2 inputs, where N is an arbitrary integer of at least 1, which will result in more than 2 inputs.

With respect to independent claim 1, the Examiner also alleged that the language "at most" simply requires that a reference teach an embodiment with no more than the disclosed number. Applicants respectfully submit that claim 1 was previously amended to delete the language "at most" in an Amendment filed on July 2, 2004. Therefore, the references require teaching an embodiment with more than the disclosed number since the claim presently recites an instruction that includes N+2 inputs, where N is an arbitrary integer of at least 1.

Also with respect to independent claim 1, the Examiner alleged that the clause "one of the inputs is a constant" has no support in the body of the claim because the claim mentions constant data but not constants used as inputs. Applicants respectfully submit that the body of the claim recites that a constant storage device includes "a constant valid flag storage region that stores a constant valid flag representing whether a constant stored in a plurality of constant addresses are valid or invalid." Based on the number of inputs, one of the inputs is a constant that is stored in the constant storage device. The inputs are data in the instructions (for example, please see specification at page 14, line 30 – page 16, line 8).

In view of the reasons given above, Applicants respectfully submit that Yumoto et al. do not disclose or teach the recitations of claim 1, and the rejection of claim 1 should be withdrawn. Applicants also respectfully submit that the rejection of dependent claims 2-9, 11 and 12 should be withdrawn for at least the same reasons given above with regard to respective base claim 1.

Applicants respectfully submit that the rejection of independent claim 13, which also recites "a handled instruction that includes N + 2 (N is an arbitrary integer of at least 1) inputs, in which one of the inputs is a constant when an instruction has N + 2 inputs," should be withdrawn for the same reasons given above with regard to independent claim 1. Applicants also respectfully submit that the rejection of dependent claims 14-17, 19 and 20 should be withdrawn for at least the same reasons given with regard to respective base claim 13.

Conclusion

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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